Improved Start-Up Performance for Charge Pump TPS6030x

Thomas Schäffner *Power Management Low Power*

ABSTRACT

This document shows a solution to enhance the start-up performance of the TPS603xx charge pumps. With the circuitry shown, the device can drive at start-up into full load (40 mA).

The TPS603xx charge pumps consist of two charge pump stages that operate in series. The first one is an unregulated doubler charge pump with its output OUT1. It supplies a second regulated charge pump which provides 3.3 V or 3 V respectively at OUT2. Therefore, the first charge pump must be able to provide twice or 1.5 times the output current of the second one, which works in either a x2 or x1.5 conversion mode. This means that the input voltage of the second charge pump stage is either doubled or increased by a factor of 1.5.

However, at start-up, the output current of the first charge pump is limited to typically 2 mA until the output voltage at OUT2 reaches its nominal value. This is because the internal circuits use the output voltage of OUT2 as supply voltage. At start-up the lower voltage from the input is used, which limits the start-up performance.

The document shows a solution to enhance the start-up performance. With this circuitry the device can drive at start-up into full load (40 mA) at OUT1.

NOTE: When OUT1 is loaded with 40 mA, OUT2 must not be loaded.

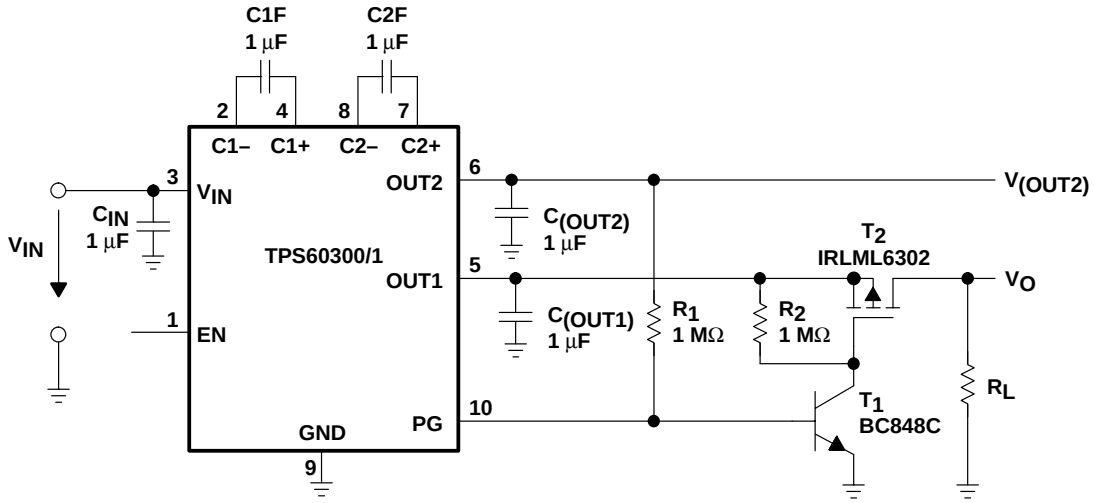

Figure 1. Schematic for Improved Start-Up at OUT1

Figure 1 shows the circuit consisting of the TPS6030x charge pump and two external transistors. The schematic is shown for the open drain power-good version. If the push-pull power good version is used, R1 must be connected between the power good output and the base of T_1. The value of T_1 should then be in the 100 kΩ range.

Figure 2 shows the timing diagram for start-up. With the device enabled, the voltage at OUT1 and thereby the voltage at the source pin of T_2 rises to about 2 x V_I. When the output voltage at OUT2 reaches its nominal value, the power good output (PG) becomes high and T_1 begins to conduct. T_1 pulls the gate of the PMOS transistor T_2 to GND, switching on T_2 and providing the output voltage at pin V_O. Channel 2 in Figure 2 shows the output current rising immediately to 40 mA. In order to minimize losses, a low VT, low-voltage PMOS transistor (IRLML 6302) has been used for T_2.

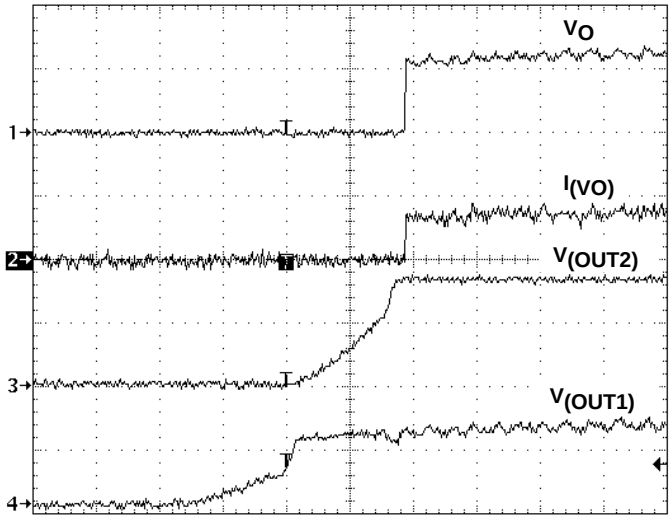

Figure 2. Start-Up Timing

Free samples can be ordered from **http://www.ti.com**. Type in the complete device name in the quick search box and select *check stock* or *order* under *Availability/Samples*. To get more detailed information about the device, see the TPS6030x data sheet (literature number SLVS302).

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265